2020 32nd International Conference on Microelectronics (ICM) Program

Monday, December 14

Monday, December 14 10:00 - 11:00

Tutorial-I: Security and Trust: the Internet of Things (IoT) World

By Nicolas Sklavos, SCYTALE Group,
Room: Virtual Room-I

Monday, December 14 11:00 - 12:00

Tutorial-II: Hardware emulation of memristor devices

Stavros G. Stavrinides & Rodrigo Picos
Room: Virtual Room-I

Monday, December 14 1:00 - 2:30

Tutorial-III: Emulation: a key acceleration platform for SoC development and verification

By Fadi Obeidat, Cadence
Room: Virtual Room-I

Monday, December 14 3:00 - 5:00

Panel Session: Challenges of Entrepreneur and Startup

Room: Virtual Room-I

Tuesday, December 15

Tuesday, December 15 10:00 - 10:30

OpCer: **Opening Ceremony**

Room: Virtual Room-I

Tuesday, December 15 10:35 - 11:35

Keynote Speaker I: Doing Research in Knowledge-based Societies

Prof. Franco Maloberti
Room: Virtual Room-I
Chair: Abdallah Kassem

Tuesday, December 15 11:45 - 1:00

S11: Complex systems

Room: Virtual Room-I
Chairs: Issa Etier, Hassan Mostafa

Energy Management Strategy for Grid Connected DC Hybrid Micro Grid Using Particle Swarm Optimization Technique
Abdelrahman Salem, Ahmed El-Shenawy and Mostafa S. Hamad
Energy management for micro-grids is a vital issue for the control system. Proper control system should fulfill load demands and ensure system stability with the minimum cost. This paper presents an energy management strategy (EMS) for grid connected DC hybrid micro-grid with cost minimization while considering the dynamics of renewable sources. Modified particle swarm optimization (MPSO) is used to solve the energy management optimization problem. Genetic algorithm (GA) is also used to verify the MPSO result. Hierarchical control is used to combine the optimization technique within the control system to achieve optimum performance.

Highly-Reliable Approximate Quadruple Modular Redundancy with Approximation-Aware Voting
Mahmoud Saleh Masadeh, Alain Aoun, Osman Hasan and Sofiene Tahar
Redundancy has been a general method to produce a fault-tolerance system. The Triple Modular Redundancy (TMR) with majority voters covers 100% single fault-masking, where the minimum area overhead is 200%. On the other hand, approximate computing is suitable for applications that can tolerate errors and imprecision in their underlying computations. Thus, inexact results allow reducing the computational complexity and hardware requirements with increased performance and power efficiency. This work explains how approximate computing could provide low-cost fault-tolerant architectures with an enhanced system's reliability. In particular, we implement a novel Quadruple Modular Redundancy (QMR) designs using three identical approximate modules in addition to the exact module. Moreover, a two-steps magnitude-based voter is proposed to be able to

tolerate approximation error. To validate our approach, we conducted experiments and the results showed the ability to achieve high fault-tolerance, i.e., 99.88%, while reducing the probability of system failure by 15%, with 62% and 49.5% reduced area and power, respectively, compared to the traditional TMR.

Trajectory Planning in Cooperative Robots Using Artificial Vision

Abel A. Rubin, Gregoria Corona, Fernando Reyes-Cortes and José E. M. Gutiérrez-Arias

When obtaining a mathematical model of any physical system, it is very desirable to be able to verify it before making its implementation, for it several methods are resorted to, one of them is the simulation. In this work we present a system of two mobile robots differential type one considered as leader or slave and the other as follower. The leader robot is designed in SolidWorks to export it to the software of MATLAB where it enters its kinematic model in SIMULINK, to carry out a simulation validating the model to finally carry out its implementation. A PID control is applied to the leading robot in the speed of each of the wheels to make the trajectory, while a machine vision system implemented in the slave robot allows to follow the leading robot, so that the path is traveled in a collaborative way.

A Novel Method for E. Coli Contamination Detection in Underground Water

Sahar Kamand, Ali Hage-Diab and Ali Al Khatib

Microbial water contamination is a serious issue facing developing countries, especially Lebanon. It causes dangerous health risks and diseases such as Cholera. Currently, no real time test is available that can give immediate results about water microbial contamination, but without the need for reagents or high maintenance components. We worked on a new idea that can help in developing such a test to be used for the design of a real time water contamination alert device. The hypothesis we aimed to validate was that light absorbance in bacteria contaminated water sample differs before and after heating. Samples of distilled water were contaminated with cultured E. coli. Light absorbance of wavelength ranging from 205 to 600 nm was measured, using a spectrophotometer, before and after heating to 80 °C. The most promising results showed an average of approximately 15% difference in absorbance (using 550 nm wavelength). These promising results can be used to develop a fully automated device to be put near water springs in order to detect the real-time presence of E. coli as an indicator of biological contamination. A specialized circuit can be designed to control an automated testing device that samples the water and tests it. Contamination test results can be sent via network communication to a remote sensing center for early disaster warning.

Low-Cost FMCW Radar Human-Vehicle Classification Based on Transfer Learning

Ali Rizik, Andrea Randazzo, Roberto Vio, Alessandro Delucchi, Hussein Chible and Daniele D. Caviglia

Detection and classification of moving targets is an essential feature in many applications like road surveillance systems, autonomous cars, and smart gate systems. Multi-chirp sequence Frequency Modulated Continuous Wave (FMCW) radars with a 2D FFT processing can be used to produce a Range-Doppler images (R-D maps) containing the signature of the target. However, in low-cost FMCW radars, these images suffer from many problems like low-resolution and ambiguity. Such problems can make the image look unrealistic as well as hard to process and classify. In this paper, we propose a human-vehicle classification method based on Transfer Learning. The classification is done by processing the R-D maps generated by a low-cost short range 24 GHz FMCW radar with a convolutional Neural Network (CNN).

The adopted CNN succeeded to reach a 96.5% accuracy in discriminating humans from vehicles.

Tuesday, December 15 1:00 - 1:30

LB1: Lunch Break

Room: Virtual Room-I

Tuesday, December 15 1:35 - 2:25

S12: CAD/Analogue Systems

Room: Virtual Room-I

Chairs: Anas N. Al-Rabadi, Mustapha Hamad

A 26.24uW 9.26-ENOB Dynamic RAM Based SAR ADC for Biomedical Application

Ola Ibrahim, Rana Hesham and Ahmed Soltan

This work introduces a new successive approximation register circuit (SAR) for SAR analog to digital converter (ADC) based on Dynamic Random Access Memory (DRAM) cells. Based on the proposed DRAM based SAR ADC and a differential capacitive DAC, a 10-bit 2V ADC is designed in 0.18um CMOS technology. The proposed SAR is compared to traditional SAR to verify that the proposed SAR decreases the power of SAR ADC for biomedical applications. The power consumption for the proposed SAR ADC is found to be 26.24uW with ENOB equal to 9.26, and the maximum sampling frequency is 1MHz. For the traditional SAR ADC the power consumption is 43.56uW and ENOB is 9.3.

Design of Multiplicative Inverse Value Generator Using Logarithm Method for AES Algorithm

Goh Yie Yen, Siti Zarina Md Naziri, Mohd. Nazrin Md Isa, Razaidi Hussin and Rizalafande Che Ismail

Advanced Encryption Standard (AES) algorithm is one of the most widely used symmetric block cipher that is utilized in the protection of data through symmetric cryptography algorithm, as it offers high efficiency and ability in securing information. In AES, the SubByte/InvSubByte transformation costs an amount of memories for the lookup tables (LUT) that leads to area usage in hardware. As per mathematical equations, the SubByte/InvSubByte is able to share the same resource which is the multiplicative inverse value table. Instead of using LUTs, the multiplicative inverse values can be generated on-the-fly as needed. Therefore, this paper presents the custom hardware design and implementation of multiplicative inverse value generator using logarithm method specifically for AES algorithm. The logarithm method benefits the usage of antilog and log values in obtaining the multiplicative inverse value. The EDA tools as Altera QuartusII, Synopsys Design Compiler and IC Compiler are used to perform functional simulation, on synthesis analysis and block-level implementation. Detailed comparison is made between this work and previous implementation. The newly designed multiplicative inverse value generator has achieved the improvement on speed and area as compared to previous implementation. The area of the design is reduced around 8.5% with current improvement of 63.091 μm2, while the speed has increased to 2.54 ns with a positive slack of 0.11 ns, which is shorter than the

previous implementation. The new design also outreached the performance of the common LUT-based design.

Comparative Study of Evolutionary Algorithms for a Hybrid Analog Design Optimization with the Use of Deep Neural Networks

Ahmed Mohamed Elsiginy, Eman Azab and Mohamed Elmahdy

Analog design optimization is the process of optimizing the circuit parameters to achieve specific performance metrics. In order to choose the best optimization methodology, a comparative study between different methodologies is needed. This work introduces hybrid design optimization method that combines Evolutionary Algorithms (EA) such as Particle Swarm Optimization (PSO) or Genetic Algorithm (GA) with a multioutput Deep Neural Network (DNN) to obtain both fast and accurate circuit optimizer. A CMOS Miller op-amp is used as an example of the optimization problem. Training data for the DNN is extracted with Mentor Analog Fast Spice (AFS) and using TSMC 90nm PDK. This work gives important insights on how to choose the best DNN structure by showing that using Adadelta optimizer in the DNN training phase is the best compared to Adagrad and Gradient Descent(GD). Moreover, it is proven that there is an optimum size of the DNN to achieve the least prediction error. Finally, a comparative study between PSO and GA algorithms proved that PSO has less failure rate for all test iterations.

Tuesday, December 15 2:30 - 3:30

KS2: CMOS-Compatible Piezoelectric MEMS for Fluidic and Acoustic Applications

Prof. Ulrich Schmid

Room: Virtual Room-I

Chairs: Abdallah Ababneh, Ahmed Madian

Tuesday, December 15 3:40 - 5:00

S13: Biomedical Engineering - Bio-Informatique-I

Room: Virtual Room-I

Chair: Omar Falou

MATLAB/Simulink Mathematical Model for Lung and Ventilator

Mohammad Jaber, Lara Hamawy, Mohamad Hajj-Hassan, Mohamad Abou Ali and Abdallah Kassem

Patients diagnosed with positive coronavirus results suffer from difficulties in breathing and major drop in blood oxygen saturation. This could lead unfortunately to a possible death if not treated well. Thus, this has increased the demand for the medical mechanical ventilators worldwide. The idea behind this work is development of a computational model for the study of the impact of different ventilation modes on patient's respiratory system generally, and lungs more specifically. This model has been created using Matlab/Simulink platform. The studied ventilation mode is the Pressure Controlled Ventilator (PCV) signal combined to single and two compartmental models in series and in parallel mathematical models configuration of the lungs that represent the respiratory system parameters for testing. The ventilator's setup includes the following parameters: positive end-expiratory pressure (PEEP),

pressure wave, respiratory rate (RR), tidal volume, and others. By changing one of these parameters, we can monitor how this will affect the lungs by checking the volume, flow and PV loop for each lung mode. Simulation results have been recorded and are promising because this allows to study any type of ventilation modes conventional or novel ones virtually without the need to jeopardize the life of human subjects during clinical trials.

MATLAB/Simulink Medical Fluid Pump Model with a Flow PID Controller

Abdulhalim Mohamad, Mohamad I.C. HajjHassan, Mohamed Wadaane, Ahmad ElSayed, Hussein Mohamad Wehby, Mariam Khayreldeen, Ahmed N. Al-naggar, Saeed Bamashmos, Mohamad Hajj-Hassan, Hassan Wehbi, Mohamad Abou Ali and Abdallah Kassem

Minimally invasive surgeries are one of the fastest growing medical fields today because of patient benefits such as faster recovery and reduced risk of infection. However, minimally invasive surgeries are quite challenging for the surgeon to perform because of reduced maneuvering space and visibility. As a result, more and more technological solutions are developed to aid the surgeon in this task. Medical fluid pumps are designed to: improve the visibility, control flow, maintain the pressure in operating cavity, and prevent fluid uptake that can, in severe cases, be fatal for the patient. In this paper, Simulink/Simscape medical fluid pump model has been developed. This model includes the following components: sensors (flow & pressure), speed and current controller DC motor, Dc motor driver, DC motor, Gear box, fixed displacement pump, and flow Proportional Integral Derivative (PID) controller. Finally, simulation was made and promising results have been achieved.

Patient Specific Epileptic Seizures Prediction Based on Support Vector Machine

Abdallah Gabara, Retaj Yousri, Darine Hamdy, Michael Hany and Hassan Mostafa

Throughout the last decades there has been an increasing interest in analyzing the EEG signals of epilepsy patients in order to relate it to epilepsy seizure onsets. Previous research papers were published exploring the possible techniques to utilize the EEG signals for detecting and predicting seizure onsets through Machine Learning and Deep Learning models, such as Support Vector Machines and Convolutional Neural Networks. The aim of this work is to build Machine Learning classifiers capable of predicting the seizure onsets prior to their occurrences with high sensitivity and accuracy, yet that are practically implementable on hardware. The classification method proposed involves removing certain channels for each patient, extracting the features from the EEG signal, selecting the best feature combination for each patient, and finally training the selected SVM classifier accordingly. Evaluating the performance of the proposed classification technique yields promising results for the selected patients with accuracies exceeding 95%.

Design and Implementation of Smart Shoes for Blind and Visually Impaired People for More Secure Movements

Roy Abi Zeid Daou, Jeffrey Chehade, Georgio Abou Haydar, Ali Hayek, Josef Boercsoek and Javier Serrano

Blind and visually impaired people encounter many challenges in their mobility and navigation. Their daily activities are obstructed due to their inability to adapt or identify accurately their surroundings which becomes the main reason of accidents, falling off, and getting lost in unknown areas. In this paper, the design, the implementation and the validation of smart shoes that would serve as an effective solution for more secured movements for blind and visually impaired people will be proposed. This system is developed

to detect obstacles, wet floor and patients' falls. In case of presence of one of the above incidents, the user will be notified acoustically using some voice alarms. Moreover, a compatible phone application is designed to notify the patient's parents in case of any issue and share his location. As the system is dealing with human health, some safety measurements were taken into consideration in the design phase, mainly electrical safety, in order to reduce error and false alarms as well as to increase accuracy. The system was tested over five subjects and the results have shown low faulty errors and good accuracy and detection percentages along with an accuracy that reached about 96%.

Analysis and Synthesis of Respiratory Rate for Female Patients

Muhammad Sana Ullah and Edder Mendoza

In this paper, a new method for estimating the respiratory rate (RR) signal using pulse oximeter is proposed. The PPG signal acquired from female patients is composed by three main elements which are the PPG signal itself, the motion artifacts and the respiratory rate. This paper analyzes eight (8) female patients from the Beth Israel Deaconess Medical Centre in Boston. The information (data) is collected from 'physionet.org'. The PPG normally has a significant amount of power ranging from 0 to 10 Hz and the motion artifacts are around 0 to 0.5 Hz. Therefore, the first step is to remove the motion artifacts and then extract the RR from rest of the PPG+RR signal. A record of 480 seconds (8 minutes) is analyzed from each female patient. All operations are performed in time domain digital signal processing. The algorithm performs several operations using median and moving average filters to estimate the RR component. The results give an efficiency of 96.5% considering an average error of +/-0.62 breathes per minute.

Tuesday, December 15 5:10 - 6:30

S14: Biomedical Engineering - Bio-Informatique

Room: Virtual Room-I

Chair: Nabil Karami

Variable Gain Amplifier Based on MIFGMOS Transistor for Biomedical Applications

Ibrahim L Abdalla, Fathi A. Farag and Mohamed Farhat Ibrahim

this paper introduces a method for designing a fully balanced Variable Gain Amplifier (VGA) depending on a trans-conductance variation and switched feedback resistance. In this method, the Floating Gate MOS transistor is used as a variable current source. Consequently, the trans-conductance of the gain MOS transistor is varying which is affecting the overall gain. Switching feedback resistance, varying current which in turn affects the gain range. The proposed strategy is suitable for low voltage applications since the threshold voltage of the floating transistor will be adjusted. Power mitigation and linearity are developed in the variable gain amplifier stage. Simple common source and fully balanced differential VGA are considered to illustrate the concept. The VGA circuit is designed and simulated by using the 0.13µm CMOS process; the overall VGA consumes 1.3mA from a 1.8V supply. The VGA achieves gain variation depending on control voltage and feedback resistance with bandwidth up to 1MHz.

A VCO-Based Nonuniform Sampling ADC Using a Slope-Dependent Pulse Generator

Mohamed Amine Bensenouci, Mohamed Ali, Escid Hammoudi, Yvon Savaria and Mohamad Sawan

This paper presents a voltage-controlled oscillator (VCO)-based nonuniform sampling analog-to-digital converter (ADC) as an alternative to the level-crossing (LC)-based converters for digitizing biopotential signals. This work's main purpose is to provide a good signal-to-noise-and-distortion ratio at a low average sampling rate. In the proposed conversion method, a slope-dependent pulse generation block is used to provide a variable sample rate adjusted according to the input signal's slope. Simulation results show that the introduced method gives a sampling rate near to 92 Sps, while on the same MIT-BIH Arrhythmia N 106 ECG benchmark, the classic LC-based approach shows a sampling rate that is more than 500 Sps. The benefits of the proposed method are more remarkable when the input signal is very noisy. The proposed ADC achieves a compression ratio close to 4, but with only 5.4% root-mean-square difference when tested using the MIT-BIH Arrhythmia Database.

Comparative Study on Segmentation Techniques for Biomedical Images

Samar Moustafa Ismail, Mohamed Abd El Ghany and Mahmoud Khaled Elfiqi

Segmentation is one of the most useful pillars in the medical image processing field, especially for tumors diagnosis and early detection. It is the process of partitioning the image into different regions to extract the object of interest which is the tumor in this work. This paper presents a comparison between different segmentation techniques applied on brain tumor magnetic resonance imaging (MRI) images, as a case study. The techniques under comparison are Region-Growing, Active-Contour, Graph-Cut and Global Thresholding. The performance of these techniques is evaluated based on the Jaccard Index, Dice Index and the F-score, elaborating which one is more accurate than the other.

Near-Lossless Compression for Multichannel EEG Using Empirical Mode Decomposition

Biju Karunnya Sivathanu, Midhila Madhusoodanan and Christy James Jose

At present, Covid19 cases are continually being reported all around the world. There exists an extreme shortage of specialist physicians which are being reported, which in turn affects the treatment of the pandemic disaster. The health sector is forcibly being switched to telemetry diagnoses and treatments. Hence, it becomes necessary to develop an efficient compression system for transmission and storage of applications in short time with great efforts. For biomedical applications, neurologists require an efficient system which provides more accurate and error free data once the signal is reconstructed. The aim is to improve the compression ratio and minimize the reconstruction error of electroencephalographic signal, designed by a two-stage compression scheme. Here, an empirical mode decomposition technique is used to breakdown the signal. The overall compression ratio (CR) of this method is 12.5:1. The transmitted EEG signals and the reconstructed EEG signal are found to be almost same with a percentage rate of distortion of about 5.4. In comparison with other lossless compression techniques, the proposed method offers high compression rate with a minimum probability of error.

Design and Analysis of Metamaterial Inspired Wearable Antenna for 2.45 GHz ISM Band

Srilatha G, Gottumukkala Raju and Sunny Dayal

A metamaterial (MTM) inspired wearable antenna for 2.45GHz ISM band is presented in this paper. The radiating element is designed using a rectangular patch having π shaped slot, this structure resembles metamaterial like geometry. The strip line for feed is altered to match the impedance for better performance. The proposed antenna design consists partial ground and four metamaterial unit cells under the radiating element in the same plane as ground. The MTM unit cells are designed using square shaped patches with inverted U shaped slots. The metamaterial are placed on top of the jeans cloth. The MTM unit cells helped in achieving the reduction of the specific absorption rate (SAR). The performance of the proposed antenna is presented using comparative simulated analysis like reflection coefficient, VSWR, radiation patterns and other antenna parameters for without MTM and with MTM cases. The suitability of the antenna for wearable application presented with the help of simulated analysis comparison for off-body and on-body conditions.

Wednesday, December 16

Wednesday, December 16 9:00 - 10:00

S21: CNFET/Ternary Systems

Room: Virtual Room-I

Chairs: Anas N. Al-Rabadi, Rodrigo Picos

Low Power Scalable Ternary Hybrid Full Adder Realization

Mohamed Ghoneim, Amr Mohammaden, Rana Hesham and Ahmed Madian

Multi-level electronic systems offer speed and area simplicity, reducing the complexity of implementation and power dissipation. In this paper, a Hybrid ternary full adder (FA) is proposed using CCMOS, Double Pass-transistor Logic (DPL) and Pass Transistors (PTs). The proposed FA is extended up-to 64-bits to test scalability. In order to validate the proposed full adder and calculate its performance analysis, Cadence Virtuoso tool-set is used at technology 130nm with supply voltage 0.9V. An extra transistor is added to overcome the sneak path problem that was detected during the simulation. The ternary values 0, 1, and 2 are represented with 0V, 0.45V and 0.9V respectively. According to the simulation results, the proposed work shows a superior performance which could be considered a promising alternative for low power applications.

Comparative Study of CNTFET Implementations of 1-Trit Multiplier

Doaa Abdelrahman, Rawan Mohammed, Mohammed E. Fouda, Lobna Said and Ahmed G. Radwan

Ternary logic has become a promising alternative to traditional binary logic due to achieving low power consumption and reduced circuits such as interconnects and chip area. The efficiency of the multiplier circuit can be much better using a ternary logic system. Carbon nanotube field-effect transistor (CNTFET) is a promising technology as it achieves more advantages than MOSFET due to its low off-current features such as low power and high performance. This paper presents a comparative study of four implementations of a 1-trit multiplier based on CNTFET technology. The comparison is performed in terms of power, delay, and power delay product versus variation of supply voltage and temperature. The simulation results show that the proper PDP can be achieved using the transmission gate based multiplier. All the designs are implemented using the Virtual Source CNTFET (VS-CNTFET) Stanford model.

A Novel CNFET-Based Ternary to Binary Converter Design in Data Transmission

Ramzi A. Jaber, Abdallah Kassem, Ahmad El-Hajj and Ali Massoud Haidar

The limitations in binary data transmission are mainly for low speed and a notable increase in energy consumption. Whereas, Multiple-Valued Logic (MVL) has over two-valued logic to increase the speed and to reduce energy consumption. Therefore, this paper proposes a Ternary-to-Binary Converter based on Carbon Nano-Tube Field Effect Transistors (CNFETs) to be used in ternary data transmission. The proposed converter has two ternary trits as input and four binary bits as output. Logical analysis and simulation results, using the HSPICE simulator, prove the merits of the implementation compared to existing designs regarding the transistors count, propagation delay, and energy consumption.

CNTFET-Based Design of Ternary Multiplier Using Only Multiplexers

Ramzi A. Jaber, Abdallah Kassem and Ali Massoud Haidar

Multiple-valued logic (MVL) circuit has many-valued logic in each digit to lower interconnections and energy consumption over a binary logic circuit. Therefore, this paper proposes a ternary multiplier (TMUL) that reduce energy consumption in the context of low-power embedded circuits. The CNTFET-based TMUL circuit use only cascading proposed ternary multiplexer to reduce the transistors count and improve performance efficiency. Extensive simulations along with several benchmark designs using HSPICE, prove the merits of the proposed TMUL by reducing energy consumption, improving the noise tolerance, and robustness to process variations (TOX, Channel length, CNT Count, and CNT Diameter).

Wednesday, December 16 10:10 - 11:15

S22: neural Network Systems

Room: Virtual Room-I

Chairs: Mahmoud Saleh Masadeh, Nicolas Sklavos

ConvNets Architecture for Complex Mixed Analogue-Digital Simulations

Vincenzo Bonaiuto and Fausto Sargeni

The Convolutional Neural Networks (ConvNets) with its proper hierarchical structure are known as powerful image-recognition processing architecture. In particular, the ConvNets are well suited for several image processing tasks, such as image classification data set, computer vision and natural language processing. Nevertheless, the implementation of ConvNets requires a large amount of operations as the 2-D convolutional mappings that need a very large computational power. In this paper, the authors will investigate alternative hardware architectures, based on Cellular Neural Networks (CeNNs), in order to improve the overall performances

Multilayer Perceptron Analog Hardware Implementation Using Low Power Operational Transconductance Amplifier

Sherif Abden and Eman Azab

This paper presents analog hardware implementation of multilayer perceptron (MLP) using operational transconductance amplifier (OTA) that is implemented and simulated in CMOS 180nm technology with 1.8V supply. The implemented circuits using the OTA perform addition, multiplication and activation which are the needed operations for any MLP. The components count in each circuit is small which allows implementing larger circuits. These circuits are current-mode (CM) circuits which makes the addition operation very straightforward and needs no power consumption using KCL. The power consumption and bandwidth of the OTA are 6.75µW and 32 KHz, respectively.

Verification of Neural Networks for Safety Critical Applications

Khaled Khalifa, Mona Safar and M. Watheq El-Kharashi

In recent years, Neural Networks (NNs) have been widely adopted in engineering automated driving systems with examples in perception, decision-making, or even end-to-end scenarios. As these systems are safety-critical in nature, they are too complex and hard to verify. For using neural networks in safety-critical domains, it is important to know if a decision made by a neural network is supported by prior similarities in the training process.

Verifying a trained neural network is to measure the extent of the decisions made by the neural network, which are based on prior similarities in the training process. In this paper, we propose a runtime monitoring that can measure the reliability of the neural network trained to classify a new input based on prior similarities in the training set. In the training process, the runtime monitor stores the values of the neurons of certain layers, which represent the neurons activation pattern for each example in the training data. We use the Binary Decision Diagrams (BDDs) formal technique to store the neuron activation patterns in binary form. In the inference process, a classification decision measured by a hamming distance is made to any new input by examining if the runtime monitor contains a similar neurons activation pattern. If the runtime monitor does not contain any similar activation pattern, it generates a warning that the decision is not based on prior similarities in the training data. Unlike previous work, we monitored more layers to allow for more neurons activation pattern of each input. We demonstrate our approach using the MNIST benchmark set. Our experimental results show that by adjusting the hamming distance, 75.63% of the misclassified labels are unseen activation patterns, which are not similar to any stored activation patterns from the training time.

Neural Network Assisted Variable-Step-Size P&O for Fast Maximum Power Point Tracking

Rayane Hijazi and Nabil Karami

This work proposes an ultra-fast Maximum Power Point Tracking (MPPT) algorithm for Photovoltaic (PV) system. The objective is to combine the Variable Step Size Perturb and Observe (VSS P&O) algorithm and the Neural Network (NN) algorithm to rapidly track the Maximum Power Point (MPP) of a PV. The role of the NN is to propose a new starting point for the P&O algorithm on every sudden climatic variation. This will reduce the searching time required by the P&O to reach the MPP. The proposed method is verified using MATLAB-Simulink simulations. Moreover, an experimental validation is carried out using a boost-converter in conjunction with a Microcontroller based system. The performance of the proposed method is compared with the conventional P&O and the VSS P&O on MATLAB-Simulink, and then with the experimental test. The results show that the proposed method tracks faster the MPP by 3 to 7 times compared to the two other methods.

Wednesday, December 16 11:25 - 12:30

S23: FPGA Applications

Room: Virtual Room-I

Chairs: Mohamad Mroue, Tales Cleber Pimenta

FPGA Implementation of Interval Type-2 Fuzzy System Based on Nie-Tan Algorithm

Regimar Maciel, Robson Moreno, Tales Cleber Pimenta and Paloma Rizol

The Interval Type-2 Fuzzy Logic Systems - IT2FLS processors have been widely used in control processes that analyzes uncertain information. The IT2FLS presents a superior performance compared to other methods for high uncertainty applications. In real-time control applications, circuit parallelism strategies increase the number of Fuzzy Logic Inference Per Second (FLIPS). This technique demands more hardware resources compared to sequential processing, which can make it difficult to use platforms that have resource limitations. This article presents an IT2FLS architecture implementation minimizes the use of parallel

processing in the implementation in the inference engine and maintains the amount of FLIPS suitable for real-time applications. The proposed IT2FLS architecture is implemented in FPGA. It uses the type reduction circuits based on Nie-Tan algorithm. The hardware consists of two 8-bit inputs with four Gaussian membership functions for each one, sixteen rules and an 8-bit output with seven membership functions. The results of the FPGA implementation are compared with the same architecture implemented in Matlab® using the Toolbox for type-2 fuzzy.

Motor Failure Detection in FPGA-Based Fault-Tolerant Quadcopters

Hassanein H. Amer, Ramez M Daoud, Ihab Adly, Gehad Ismail Alkady and Fady Abouelghit

Quadcopters have recently become a very important component in search and rescue missions. This paper proposes solutions to several problems facing quadcopters in such missions. First, a fault-tolerant FPGA-based architecture is developed which can recover from both soft and hard failures. It is then proven through reliability modeling that this architecture has a considerably higher lifetime than a similar architecture with no fault tolerance. Second, it is shown how to use accelerometers to detect motor faults in order to improve mission decision-making.

Hardware Implementation of Floating Point Matrix Inversion Modules on FPGAs

Chetan S, Manikandan J, Lekshmi V and Sudhakar S

Matrices are employed for diversified applications such as image processing, control systems, video processing, radar signal processing, compressive sensing and many more. Finding inverse of a floating point large scale matrix is considered to be computationally expensive and their hardware implementation is still a research topic. In this paper, FPGA implementation of four different floating-point matrix inversion algorithms using a novel combination of high level language programming and model based design is proposed. The proposed designs can compute inverse of a floating point matrix up to a matrix size of 25×25 and can be easily scaled to large size matrices. The performance evaluation of proposed matrix inversion modules are carried out by their hardware implementation on a Zynq 7000 FPGA based ZED board and the results are reported.

FPGA-Based Architectures to Recover from Hardware Trojan Horses, Single Event Upsets and Hard Failures

Gehad Ismail Alkady, Maha Shatta, Ihab Adly, Hassanein H. Amer, Ramez M Daoud, Sahar Hamed and Shahenda Eid

Third-party IPs (3PIPs) may have a Hardware Trojan Horse (HTH) that escaped detection during the testing phase. This paper proposes techniques to recover from a HTH during runtime. In the context of FPGA-based systems, it will be proven that these techniques can also recover from Single Event Upsets (SEUs) and Hard Failures (HFs). Furthermore, the identity of the 3PIP with the HTH may be determined. A DE-Standard FPGA development board with Cyclone V devices was used to successfully test the proposed designs.

Wednesday, December 16 12:30 - 1:15

LB2: Lunch Break

Room: Virtual Room-I

Wednesday, December 16 1:15 - 2:30

S24: Smart sensors and sensor networks

Room: Virtual Room-I

Chairs: Yazan H. Al-Badarneh, Fadi Zghoul

Controllable OTA Slew-Rate for CMOS Image Sensor

Ola Ibrahim, Rana Hesham and Ahmed Soltan

In this work, a proposed circuit is implemented using tsmc 0.18um technology of area 16642 um 2 with supply voltage equals 5V. A proposed implementation of a controllable Operational Transconductance Amplifier (OTA) slew rate for CMOS image sensor (CIS) is proposed. The slew rate is controlled by switching between various bias circuits for the OTA. The biasing circuit controls the value of OTA biased current, which allows controlling the amplifier's characteristics. As the flicker noise in the main contributor in reducing the quality of image sensors performance. The proposed circuit allows controlling noise effect by increasing the time of reading a pixel signal(OTA slew rate). For reducing the power consumption, the bias cell can be selected regarding the signal to noise ratio (SNR) value.

Energy Efficient Clustering Protocols for WSN: Performance Analysis of FL-EE-NC with LEACH, K Means-LEACH, LEACH-FL and FL-EE/D Using NS-2

Fathima Shemim KS and Ulf Witkowski

Wireless Sensor Networks playing an important role in applications where human interaction is difficult. WSN is extensively used in real-time applications like surveillance systems, environmental monitoring systems, disaster management and health monitoring, etc. Since sensor nodes are deployed in isolated areas, recharging or replacing node batteries is difficult. So for the better performance of the network, it's important to improve network lifetime by increasing sensor nodes' energy efficiency. Data aggregation methods and energy-efficient routing algorithms have an important role in WSN to tackle the problem with network lifetime. Hierarchical energy-efficient routing protocols are trending in the WSN research field, which helps to improve overall network lifetime by increasing the lifetime of sensor nodes by minimizing the energy consumption of each node in the network. In this paper, compared and investigated the performance of the Fuzzy Logic -Network Coding-Energy Efficient (FL-NC-EE) routing protocol with the other energy efficient clustering protocols like LEACH, LEACH-FL, K Means-LEACH and FL-EE/D using NS2. The result shows that the FL-NC-EE protocol outperforms in terms of energy efficiency and network lifetime compared to the other protocols discussed in this paper.

An Energy-Efficient Temperature Sensor Using CMOS Thyristor Delay Elements

Ian Christian B. Fernandez, Maria Theresa de Leon, Anastacia B Alvarez and Marc Rosales

This paper presents a time-based method of measuring temperature using CMOS thyristors and a time-to-digital converter akin to algorithmic analog-to-digital converters. By treating time as a signal and as an abundant resource for slow-changing quantities like temperature, slow but energy-efficient topologies like CMOS thyristors could prove useful. Coupled with a TDC that does not scale exponentially with resolution, a significantly lower energy consumption is expected. Implemented in a 65nm CMOS process, this sensor system measures temperature with nonlinearity error of ±0.25 ◦ C and resolution of 0.05 ◦ C per LSB from −15 ◦ C to 30 ◦ C while using only 0.4 nJ per measurement.

Enhancement of WSN Network Lifetime

Mohammad M. Shurman, Fatima AbuAkleek and Rawaa Quraan

extending WSN lifetime is a crucial problem. Designing, developing and implementing an energy efficient protocols for WSNs is one of the most research challenges. Researchers went toward finding more efficient solutions as proposing new routing protocols or existing protocols enhancements to extend the network/batteries lifetime. In this paper, we propose an AI enhancement for the LEACH protocol using super cluster head (SCH) and integrate the proposed enhancement with Consume Power Fairly (CPF) protocol for finding the optimal path from the source to destination. Our simulation results demonstrate 40% improvement in network lifetime.

MSCLP: Multi-Sinks Cluster-Based Location Privacy Protection Scheme in WSNs for IoT

Zainab Hussien, Doaa Qawasmeh and Mohammad M. Shurman

Location privacy protection in Wireless Sensor Networks (WSNs) is an important issue to protect sensitive objects from being reached by attackers. One of the most important information in WSNs is the location of each sensor node. However, this kind of information is very attractive to the attackers for real position exposure of nodes making the whole network vulnerable to different kinds of attacks. Source location privacy is a very major problem in WSNs; since attackers can trace-back packets to reach the source nodes. In this research, we propose a Multi-Sinks Cluster-Based Location Privacy Protection (MSCLP) scheme in WSNs that divides the WSN into clusters, each cluster managed by one cluster head (CH). Each CH sends random fake packets in a loop then sends the real packet to the neighbor's cluster head using a dynamic routing method to confuse the attacker from tracing back the real packet to reveal the actual location of the source node. In addition to deploying multi sink sensor nodes to make many routing paths in the network to protect the source and the sink sensor nodes by taking in our consideration two important metrics: the energy consumption, and the delay.

Wednesday, December 16 2:30 - 3:35

S24: Special Track Cyber-physical Systems Security-I

Room: Virtual Room-I

Chairs: Ali Ismail Awad, Mwaffaq Otoom

A High-Speed KECCAK Architecture Resistant to Fault Attacks

Hassen Mestiri, Imen Barraj and Mohsen Machhout

The hash KECCAK algorithm has been proposed by the cryptographic architect with the goal to improve the hash security and the design hardware performances. The KECCAK hash algorithm has been implemented in the cryptographic circuits to ensure the hash security. It is become the standard hash algorithm used to determinate the information integrity. To protect the KECCAK hardware implementation against the fault attacks, a few numbers of fault detection schemes have been proposed. The fault attacks consist to create an erroneous KECCAK message to extract the hash secure data. In this paper, a new fault detection scheme based on modifying the KECCAK architecture is presented where the KECCAK round is divided into two blocks. We explain the details implementation of each blocks. The security simulation results demonstrate that our scheme reaches 99.995% fault coverage. In addition,

the proposed scheme has been evaluated from viewpoint FPGA hardware implementation. The efficiency, the throughput, the frequency and the area have been evaluated and it is shown that our proposed scheme leads high frequency overhead and minimum area overhead compared to the previous work.

Hardware Security for eXtended Merkle Signature Scheme Using SRAM-Based PUFs and TRNGs

Roberto Román, Rosario Arjona, Javier Arcenegui and Iluminada Baturone

Due to the expansion of the Internet of Things (IoT), there is an increasingly number of interconnected devices around us. Integrity, authentication and non-repudiation of data exchanged between them is becoming a must. This can be achieved by means of digital signatures. In recent years, the eXtended Merkle Signature Scheme (XMSS) has gained popularity in embedded systems because of its simple implementation, post-quantum security, and minimal security assumptions. From a hardware point of view, the security of digital signatures strongly depends on how the private keys are generated and stored. In this work, we propose the use of SRAMs as True Random Generators (TRNGs) and Physically Unclonable Functions (PUFs) to generate and reconstruct XMSS keys in a trusted way. We achieve a low-cost solution that only adds lightweight operations to the signature itself, such as repetition decoding and XORing, and does not require additional hardware (like trusted computing architectures), but exploits the SRAMs found in most devices. As a proof of concept, the solution was implemented in an IoT board based on the ESP32 microcontroller.

Swarm Robotics Meets Blockchain to Deploy Surveillance Missions

Lo'ai A. Tawalbeh

Swarm Robotics can be used in many applications. But they suffer from certain limitations that make them undesirable in Surveillance applications. Among their limitations is the absence of scalability and security. Currently, these robots do not have framework that allows it to communicate with each other to execute missions autonomously and transparently. Blockchain is the new technology for distributed autonomous systems by providing set of computer nodes for data storage and distribution among the nodes in the system. Each participating node can protect and validate the data in the blockchain system. No modifications can be performed on the data records due to the fact that it is been watched by all the users. Based on the blockchain features, we focus on this research how blockchain applications can make swarm robots securely connected using Ethereum smart contracts. Starting with surveillance missions deployment task, we propose a decentralized application (DApp) for that. Then, blockchain is used by the swarms to establish the Ethereum private networks that allows them to communicate and carry out tasks. We set a test swarm robotics system and evaluate the blockchain for its performance, scalability, recoverability, and responsiveness. In conclusion, we found that blockchain enables a swarm to be globally securely connected, but there are still need for performance enhancement.

Fractional-Order Image Segmentation for Security Surveillance

Samar Moustafa Ismail

The enhancement of image processing techniques related to security surveillance issues is considered a pressing demand nowadays. Everything is now documented by digital images, out of which important information is extracted. In this work, fractional-order edge detection filters are employed in edge-based Active Contour segmentation technique for noisy surveillance images. The fractional-order filters add extra degree of freedom, allowing more

details to be detected in images, and enhancing the quality of segmented noisy images. Two types of noise, Salt and Pepper noise as well as Gaussian noise, are applied to test the noise performance of the presented segmentation technique. The superiority of the fractional-based segmentation over the conventional integer-based one was proven visually and numerically using peak signal to noise ratio for both types of noise.

Wednesday, December 16 3:45 - 5:00

S25: Special Track Cyber-physical Systems Security-II

Room: Virtual Room-I
Chair: Karim Abdellatif

Optimized Random Forest Model for Botnet Detection Based on DNS Queries
Abdallah Moubayed, MohammadNoor Injadat and Abdallah Shami
The Domain Name System (DNS) protocol plays a major role in today's Internet as it translates between website names and corresponding IP addresses. However, due to the lack of processes for data integrity and origin authentication, the DNS protocol has several security vulnerabilities. This often leads to a variety of cyber-attacks, including botnet network attacks. One promising solution to detect DNS-based botnet attacks is adopting machine learning (ML) based solutions. To that end, this paper proposes a novel optimized ML-based framework to detect botnets based on their corresponding DNS queries. More specifically, the framework consists of using information gain as a feature selection method and genetic algorithm (GA) as a hyperparameter optimization model to tune the parameters of a random forest (RF) classifier. The proposed framework is evaluated using a state-of-the-art TI-2016 DNS dataset. Experimental results show that the proposed optimized framework reduced the feature set size by up to 60%. Moreover, it achieved a high detection accuracy, precision, recall, and F-score compared to the default classifier. This highlights the effectiveness and robustness of the proposed framework in detecting botnet attacks.

Detecting Botnet Attacks in IoT Environments: An Optimized Machine Learning Approach
MohammadNoor Injadat, Abdallah Moubayed and Abdallah Shami
The increased reliance on the Internet and the corresponding surge in connectivity demand has led to a significant growth in Internet-of-Things (IoT) devices. The continued deployment of IoT devices has in turn led to an increase in network attacks due to the larger number of potential attack surfaces as illustrated by the recent reports that IoT malware attacks increased by 215.7% from 10.3 million in 2017 to 32.7 million in 2018. This illustrates the increased vulnerability and susceptibility of IoT devices and networks. Therefore, there is a need for proper effective and efficient attack detection and mitigation techniques in such environments. Machine learning (ML) has emerged as one potential solution due to the abundance of data generated and available for IoT devices and networks. Hence, they have significant potential to be adopted for intrusion detection for IoT environments. To that end, this paper proposes an optimized ML-based framework consisting of a combination of Bayesian optimization Gaussian Process (BO-GP) algorithm and decision tree (DT) classification model to detect attacks on IoT devices in an effective and efficient manner. The performance of the proposed framework is evaluated using the Bot-IoT-2018 dataset. Experimental results show that the proposed optimized framework has a high detection

accuracy, precision, recall, and F-score, highlighting its effectiveness and robustness for the detection of botnet attacks in IoT environments.

A Security Qualification Matrix to Efficiently Measure Security in Cyber-Physical Systems

Andreas Aigner and Abdelmajid Khelil

Implementations of Cyber-Physical Systems (CPS), like Internet of Things, Smart Factories or Smart Grid gain more and more impact in their fields of application, whereas they extend the functionality and quality of the offered services dramatically. However, the coupling of safety-critical embedded systems and services of the cyber-space domain introduce many new challenges for system engineers. One of these can be found in the overall level of security throughout the CPS. It is a must to achieve a high-level of security, as vulnerabilities and threats may lead to a non- or maliciously modified functionality of the CPS, which could ultimately cause harm to life of involved actors, or at least sensitive information can be leaked or lost. Therefore it is essential, that system engineers are aware of the level of security of the deployed CPS. For this, security metrics and security evaluation frameworks can be utilized, as they are able to quantitatively express security, based on different measurements and rules. However, existing security scoring solutions may not be able to generate high-quality security scores for CPS, as they do not take the special characteristic, like the communication of heterogeneous systems of physical- and cyber-space domain in an unappreciable manor, into account. Therefore, we aim to elaborate a security analysis framework, called Security Qualification Matrix (SQM), which main ideas are defined according to the structure and dependencies of CPS. We define several matrices, which are hierarchically ordered and provide security scores for each other on different levels and dimensions. Overall, the SQM framework proves a flexible and straight-forward concept to express the level of security in CPS by considering all present systems, attacking scenarios, as well as mitigation concepts.

DNSSEC as a Service - A Prototype Implementation

Visham Ramsurrun, Amreesh Phokeer, Amar Seeam, Panagiota Katsina and Sumit Anantwar

Domain Name System (DNS) plays a massive role in today's technological era. While initially designed to facilitate communications over the Internet and over networks, the DNS in itself is not secure enough considering the type and criticality of information being shared today. Considering its worldwide acceptance and popularity, securing the DNS without breaking its operation has become vital. DNSSEC is seen as a viable option. However, its adoption rate is not encouraging. Research shows that complexity associated with currently proposed solutions were major turn off for organizations. This paper proposes the creation of a DNSSEC signing service whereby customers register themselves with the service provider and the latter deploys a signing environment for them which includes a DNSSEC signer, a database and web services for access purposes. Customers will only have to use the web services to create and manage their zones and the zone signing can be done automatically or with a simple click of a button. Signed zones are sent back to customer authoritative DNS servers securely using TSIG and incoming DNS requests are signed. This solution involves open-source tools and service providers make use of Linux containers for customer environment and space for resource efficiency. All the complexity and additional maintenance involving the system are taken off the customer's shoulders and managed by the provider while also facilitating their tasks through GUI operations.

High Throughput Pipelined Implementation of the SHA-3 Cryptoprocessor

Argyrios Sideris, Theodora Sanida and Minas Dasygenis

Today, in the modern world of digital communications, sensitive information is transmitted via public networks. So it is essential to ensure the privacy of their transmission with confidentiality, security and integrity using techniques like hashing. An optimized and high throughput implementation of Secure Hash Algorithm-3 (SHA-3) in hardware is a vital issue for the efficient operation of many modern and demanding systems that utilize this operation in high bandwidth links. In this paper, we propose a pipelined architecture of the SHA-3 256 algorithm in order to increase the hash function calculation speed in Field Programmable Gate Array (FPGA). The proposed architecture is able to function in both single block and multi block messages. Our design is described in Very High Speed Integrated Circuit Hardware Description language (VHDL) and synthesized in FPGA Arria 10 GX. The results show that a significant improvement in throughput, frequency and efficiency is achieved compared to the published literature.

Thursday, December 17

Thursday, December 17 9:00 - 10:00

Keynote Speaker III: Cellular and Connectivity Circuits & Systems; the road ahead

Prof. Osama Shanaa
Room: Virtual Room-I
Chair: Jad G. Atallah

Thursday, December 17 10:10 - 11:20

s31: Semi-Conductor Systems-I

Room: Virtual Room-I
Chairs: Pankaj Arora, Hani Jamleh

A Low-Power 0.4-2.3GHz NB-IoT UE Receiver with -15dBm OOB-Tolerant RF Front End

Hassan Ali, Ahmed Nader and Mohamed Aboudina

This paper presents the system and circuit level design of a NB-IoT receiver (RX) based on 3GPP Technical Specification (TS) 36.101. This design targets serving many NB-IoT operation bands, so no off-chip filter is used. This dictates large linearity specification on the RF front end to avoid desensitization by -15dBm out-of-band blockers (OOBs). Large linearity specification leads to large power consumption. A solution is proposed to reduce power consumption of the RF front end, while achieving high gain and high linearity. The proposed RF front end provides 29.5dB gain and -10.9dBm IIP3 while consuming 2mW from a single 1.1V power supply. The solution includes adding gain programmability to conventional resistive feedback LNA to relax the trade-off between linearity and power consumption. The RF front end is designed using a 40nm CMOS technology and occupies an area of 0.2mm 2 .

New Proposed Methodology for Radiation Hardening by Design of MOS Circuits

Hesham Hassan Hassan, Mohammed Amin and Serag E. D. Habib

One of the radiation effects on ICs is the Total Ionizing Dose (TID) effects. TID effects are accumulative effects that build up during the exposure time and may cause a functionality failure for the exposed ICs. In this paper, we propose a new systematic methodology for developing a predictive TID-aware models for bulk FETs. TID-aware models developed using our methodology enable circuit designers to predict the expected worst case performance degradation of their circuits if exposed to high radiation doses.

Role of Material Gate Engineering in Improving Gate All Around Junctionless (GAAJL) MOSFET Reliability Against Hot-Carrier Effects

Hichem Ferhati, Fayçal Djeffal and T Bentrcia

In this paper, dual-material gate engineering aspect is proposed as an efficient way to address the Gate All Around Junctionless (GAAJL) MOSFET devices immunity against hot-carrier effects (HCEs). Analytical models concerning the device analog/RF performance metrics including the degradation related to HCE are developed, where a good agreement

with TCAD-based numerical data is recorded. The impact of the defects induced by HCEs on the device analog performance is thoroughly analyzed. Interestingly, promising design strategy based on combining Multi-Objective Genetic Algorithms (MOGAs) with gate engineering paradigm was adopted for bridging the gap between analog/RF performance and improved reliability against HCEs. Moreover, this systematic study has enabled exciting possibilities to the designer for acquiring a comprehensive review regarding the GAAJL MOSFET design reliability-analog/RF performance tradeoffs. Therefore, the proposed design methodology offers a sound pathway to designing high-performance and reliable transistors strongly desirable for nanoelectronic applications.

An ULP Capacitor-DAC-Based Constant-Slope Digital-To-Time Converter

Kareem Rashed, Omar Hassan, Mohamed Aboudina, Ahmed Nader and Faisal Hussien

This paper presents a constant-slope digital-to-time converter (CS-DTC) that leverages the concepts of constant-slope charging and charge redistribution to achieve high linearity with ultra-low power consumption (ULP) that makes the proposed DTC suitable for the Internet-of-Things (IoT) applications. The proposed CS-DTC is designed and simulated in 40-nm technology. It draws 8 µA from a 1.1 V supply when clocked at 50 MHz while achieving 3.7 pS resolution over a 7-bit range. A differential nonlinearity (DNL) and an integral nonlinearity (INL) about 0.2 LSB and 0.3 LSB, respectively, are achieved.

Thursday, December 17 11:30 - 12:30

s32: Semi-Conductor Systems-II

Room: Virtual Room-I

Chair: Fouad El Haj Hassan

A Fully Integrated 1.2V LDO Regulator

Khaldoon Abugharbieh, Basel Yaseen and Abdullah Deeb

This work presents a fully integrated low-drop out voltage regulator that achieves a fast-transient response by utilizing two feedback mechanisms. The first feedback mechanism is an analog regulation that includes an error amplifier. The second feedback mechanism is based on digitizing any fast change in the output voltage using multiple comparators and subsequently enabling either an NMOS based or a PMOS based current DAC. The DAC provides current in opposite polarity to the sharp transient change in load current. As a result, sharp changes in load current is addressed by high-speed current DACs and is not limited by the performance of the error amplifier. The LDO was implemented using 180nm CMOS technology devices. It uses a supply voltage input range of 1.6 V - 2.0 V and produces an output voltage of 1.2 V. In simulations, the LDO regulator achieves 188 uA quiescent current, -56 dB PSRR @ 1 KHz noise frequency and an output voltage drop of around 200 mV for a load current step of 100 mA.

Stacked Nanosheet Based Reconfigurable FET

M Ehteshamuddin, Sajad A. Loan and M Rafat

In this paper, we present a vertically stacked (VS) nanosheet (NS) FET architecture that can realize device reconfigurability and inverter action at the device level of operation. NS are uniformly n + and p + doped as in the junctionless device, which then is combined with the stacked silicides at the drain end to perform complimentary operation. A single gate with

GAA architecture provides improved electrostatic integrity. With proper biasing, the device operates as nFET and pFET, respectively. Further, the impact of L g and NS thickness scaling on device characteristics are also analyzed. We observe that at reduced NS thickness, much improved OFF-state device characteristics along with the gain margin in VTC curve is obtained, due to efficient gate control of the channel region.

Digital-LDO Switched Capacitors Based for 0.5V Applications

Thiago Alves Mendes do Amaral, Hugo Daniel Hernandez and Wilhelmus Van Noije

This work presents the design of a 0.5V digital low dropout voltage regulator (DLDO) in 180nm CMOS technology for Dynamic Voltage Scaling applications. Dynamic and leakage power consumption in VLSI systems are effectively reduced by ultra-low voltage operation, being that the maximum energy efficiency is achieved at supply voltage below 0.5V. Feedback-controlled analog LDO based on an operational amplifier can fail if it operates at sub/near-threshold voltage. Digital LDOs have potential to replace the analog circuits in the feedback loop for a digital equivalent, which enables ultra-low voltage operation. An efficiency peak of 98%, an steady-state error lower than 7mVp was achieved by post-layout simulations for a load current range from 100µA to 1.25mA.

GPS Receiver Frontend Design for Radio Frequency Interferences and Noise Cancellations

Wen Cheng Lai

This article proposes integrated GPS receiver frontend design, performance optimization and low power dissipation. The proposed frequency synthesizer with a cross coupled negative-resistance multiple-gated circuit (NRMGC) voltage-controlled oscillator (VCO) by employing a transformer-based LC-tank achieves low phase noise. The proposed design chooses decoupling effect to decrease coupling inductances and then decrease quality factors to obtain higher oscillation frequency and wide tuning range. The eye pattern measured results demonstrate that receiver frontend for radio frequency interferences achieves optimized GPS (global positioning system) performance.

Thursday, December 17 12:30 - 1:15

LB3: Lunch Break

Room: Virtual Room-I

Thursday, December 17 1:15 - 2:50

S33: Fractional-Order Systems

Room: Virtual Room-I

Chair: Stavros G. Stavrinides

Analogue Realization of a Fully Tunable Fractional-Order PID Controller for a DC Motor

Georgios Pappas, Vassilis Alimisis, Christos Dimas and Paul Peter Sotiriadis

This paper explores a new integrated-circuit architecture of an analog, active, tunable and selectively fractional or integer -order PID controller using operational amplifiers. Controller's

major parameters are tuned via appropriate DC currents to the desired values. The proposed architecture is validated in a case study of a DC motor control and it can be used as a building block in industrial and commercial control systems. Circuit and physical design (layout) have been done in TSMC 90nm CMOS process. Extensive circuit and post-layout simulation are carried out using the Cadence IC design.

Analogue Realization of Fractional-Order Healthy and Cancerous Lung Cell Models for Electrical Impedance Spectroscopy

Vassilis Alimisis, Christos Dimas and Paul Peter Sotiriadis

This work proposes an integrated-circuit architecture emulating healthy and cancerous lung cell behaviors, approximated by Cole models and is suitable for calibration and phantom experimental testing of electrical bioimpedance circuits and systems. The architecture is based on fractional-order elements implemented with both active and passive components, offering an accurate transfer function behavior between 10kHz and 1MHz. The high-level architecture includes an analog all-pass filter coupled with a current conveyor. Performance and accuracy of the proposed architecture is confirmed via Monte-Carlo simulation. The proposed circuitry has been designed in TSMC 90nm CMOS process and simulated using the Cadence IC suite.

Fractional-Order Memristor Emulator with Multiple Pinched Points

Nariman Khalil, Mohammed E. Fouda, Lobna Said, Ahmed G. Radwan and Ahmed Soliman

The paper concentrates on proposing voltage-controlled first- and second-order memristor emulators. The tunable emulators are designed using an operational-transconductance amplifier (OTA) and voltage multiplier blocks plus a fractional-order capacitor. The second-order presented emulator provides two pinched points controlled by the order alpha of the employed fractional-order capacitor. Numerical and PSPICE simulation results using AD844 and AD633 are introduced for different cases to approve the theoretical findings. The experimental verification is presented, showing the design flexibility and controllability based on fractional-order parameters.

On Series Connections of Fractional-Order Elements and Memristive Elements

Nariman Khalil, Mohammed E. Fouda, Lobna Said, Ahmed G. Radwan and Ahmed Soliman

This paper proposes a current-controlled fractional-order memristor emulator based on one active building block. The emulator consists of a multiplication mode current conveyor (MMCC) block with three passive elements. Additionally, the series connection of fractional-order inductor (FOI) and fractional-order capacitor (FOC) with memristive elements in the $i-v$ plane is demonstrated numerically for different cases. Changing the order of the FOC or FOI and its effect on the pinched hysteresis loop area is investigated, which improves the controllability of the double loop area, the location of the pinched point, and the operating frequency range. Numerical, PSPICE simulation results and experimental verification are investigated for different cases to approve the theoretical findings. Moreover, a sensitivity analysis using Monte Carlo simulations for the tolerance of the discrete components of the memristor emulator is investigated.

Two-Port Network Analysis of Equal Fractional-Order Wireless Power Transfer Circuit

Dalia A. Fathi, Mohammed E. Fouda, Lobna Said, Nourhan Khafagy and Ahmed G. Radwan

Wireless power transfer (WPT) has been widely employed in many applications. Its advantages have added more safety and ease in various medical, industrial, and electrical applications. This paper investigates the two-port network concept in the analysis of the fractional-Order WPT circuit. A general expression for the WPT efficiency as a function of two-port network parameters is derived. It is represented in terms of the transmission matrix parameters of a generalized Two-Port network. The analysis is performed on both Series-series and Series-parallel topologies. The best efficiency is then found by trying different values of frequency and load. The efficiency is simulated and investigated analytically and numerically on a SS and SP topology. The SP topology's efficiency and performance are found to be better, applying equal fractional-order, which is in this paper equals 0.9.

Parameter Identification of Flexible Supercapacitors with Fractional Cuckoo Search
Amr M. AbdelAty, Mohammed E. Fouda, Menna Elbarawy, Hazem Attia and Ahmed G. Radwan
In this paper, we identify the model parameters of flexible supercapacitor from time-domain data using fractional cuckoo search. The time-domain data are five galvanostatic charging/discharging (GCD) curves of reduced graphene oxide-based flexible supercapacitor at different exfoliated-graphene-mediated graphene oxide (EGM-rGO) relative content. These time-domain curves are used the parameters of three well-known supercapacitor models: Rs-CPE, R p-R s-CP E, and R s-C-CP E. The extracted parameters are summarized, and the effect of EGM-rGO relative content is discussed. Based on these discussions, one model is recommended for each EGM-rGO relative content.

Thursday, December 17 3:00 - 4:00

S34: MEMS/Antenna

Room: Virtual Room-I
Chairs: Yanal S Faouri, Elias Nassar

Simulation of Terahertz Broadband Antennas for Rectenna Applications
Mohd Bazli Mohd Mokhar, Shahrir Rizal Kasjoo and Nurjuliana Juhari
In this paper, we designed and simulated several self-complimentary broadband antennas for the used in rectenna applications at terahertz frequencies. Rectenna consisting two-terminal planar nanodiode such as self switching diode is considered as a requirement in designing the broadband antennas. Antenna's performance is then compared in term of return loss, gain, directivity and radiation efficiency.

Design of the Millimeter-Wave Textile Antenna Loaded with AMC Structures for 5G Applications
Hamza Ben Hamadi, Said Ghnimi and Ali Gharsallah
In this work, we designed a millimeter wave textile antenna for the 28 GHz band. This antenna was tested using textile materials placed over an artificial magnetic conductor (AMC). The prototype (antenna and AMC) was fabricated on polyester substrate with a thickness equal to 0.35 mm and a size of 16.8*14.4*1.84 mm3 only. To isolate the antenna from the human body, an artificial magnetic conductor (AMC) plane was added on the reverse side of the ground plane. The simulation results obtained by simulator CST present the electrical and radiation characteristics of the proposed antenna. The comparison of the antenna without

AMC in free space and that backed by AMC showed that the latter performance is better. The proposed structure can be used in smart garments with minimized risk to human health.

High Contrast Gratings (HCG) MEMS-Tunable VCSEL Compact Model

John Jairus D.P. Eslit, Maria Theresa de Leon and Marc Rosales

High contrast grating (HCG) microelectromechanical structure(MEMS)-tunable VCSELs have advantages that make them promising for applications like optical coherence tomography (OCT), light detection and ranging (LIDAR) and dense wavelength division multiplexing (DWDM). Circuit simulator-compatible laser compact models can aid circuit designers in improving the performance of systems that use them. While a compact model for VCSEL already exists, it does not sufficiently describe the behavior of tunable VCSELs. This paper discusses the creation of a compact model for HCG MEMS-tunable VCSELs implemented in Verilog-A using semiconductor laser rate equations.

A Lumped Element Model for the Damping Mechanism of Micro-Oscillators in the Transitional Flow Regime

Tobias Zengerle, Julian Joppich, Henrik Lensch, Abdallah Ababneh and Helmut Seidel

This study presents a Lumped Element Model (LEM) for the different damping mechanisms of micro-oscillators oscillating in a gas medium near a boundary. The LEM is based on resistive and inductive components as well as on a newly introduced inductive constant phase element (CPE). The model is applied to experimental data of micro-oscillators for six different gas atmospheres and gap widths to a limiting boundary in-between 150 to 3500 µm. The LEM is in good agreement with the experimental data of the first four bending modes and the electronic components exhibit a reasonable correlation to the physical properties of the measured gases.

Thursday, December 17 4:10 - 6:10

S35: General Circuits Designs

Room: Virtual Room-I

Chairs: Majida Al Asady, Fadi R. Shahroury

Application for Automatic Placement of Hardware Modules in Layout Form

Konstantinos Velonis, Theodoros Simopoulos and George Alexiou

This work presents an application for automatically placing sub-modules of an ALU to create a layout design. This process is made as easy to use as possible by utilizing a webpage environment as the user interface. The user is offered a selection of available modules and can place them on a grid, creating a final design with the desired characteristics. This application, although a bit limited on its own, stands as a proof of concept for a future project with a bigger scope, even on the CPU core level.

Hardware Acceleration of Dash Mining Using Dynamic Partial Reconfiguration on the ZYNQ Board

Mohamed H. Abdulmonem, Jihad EssamEddeen, Michael Hany, Sayed Hanafi and Hassan Mostafa

Dynamic Partial Reconfiguration (DPR) enables reconfiguration of FPGA parts at runtime to provide flexible hardware accelerators with advantages in area, power, reconfiguration time,

and memory utilization. in this paper a design employing DPR technology is proposed to accelerate the mining of the cryptocurrency DASH using the PCAP controller on the ZYNQ 702 Evaluation Board. The DPR design remarkably reduces the area needed for implementing the hash of the mining process of dash on the ZYNQ 702 board.

Threshold Switch Modeling for Analog CAM Design

Jinane Bazzi, Mohammed E. Fouda, Rouwaida Kanj and Ahmed M. Eltawil

In this work, we develop a model for a threshold switching device to be used in the context of an analog CAM design. For this, we tune and optimize a two-terminal hysteretic device model that relies on a state variable to capture proper behavior in different operating conditions. It satisfies a 1 mV/decade ON switching slope. We study the model sensitivities in the context of device charging a capacitor and an analog CAM cell switching between match and mismatch states. We also study the impact of variations in the device hold and switching voltage parameters on the analog search interval.

Collision Probability Computation for Road Intersections Based on Vehicle to Infrastructure Communication

M. Saeed Darweesh and Mahmoud Shawky

In recent years, many probability models proposed to calculate the collision probability for each vehicle and those models used in collision avoidance algorithms and intersection management algorithms. In this paper, we introduce a method to calculate the collision probability of vehicles at an urban intersection. The proposed model uses the current position, speed, acceleration, and turning direction then each vehicle shares its required information to the roadside unit (RSU) via the Vehicle to Infrastructures (V2I). RSU can predict each vehicle's path in intersections by using the received data. By considering vehicle dimensions in our calculation, RSU will detect a possible collision point and time to collision (TTC) for moving vehicles at the intersection. Simulation results show that this model can detect collisions occurrence early, so it will decrease the probability of a collision occurs.

Mechanical Analysis of Human DBS Electrodes

Heba Draz, Eslam Elmitwalli, Mirna Soliman, Salam Gabran, Mohamed Basha, Hassan Mostafa and Amal Zaki

Deep brain stimulation (DBS) electrodes have been proved to be effective in treating neural related diseases in rodents. These devices were successfully extended to the field of human neuro therapy. Many different electrodes exist. However, no quantitative ranking criterion is available to allow meaningful comparison of the various DBS electrodes to aid the designer. This paper presents a novel Figure of Merit (FOM) dedicated to DBS electrodes. The proposed optimization performance takes into account safety factors of mechanical analysis and the estimated fabrication cost of some materials. The FOM is used to rank several DBS electrode designs. Finite Element Models (FEM) analysis for several electrode layouts are conducted. FEM shows the effects of different design parameters on the electrode mechanical performance. These parameters include electrode dimensions, geometry, and materials. The electrodes mechanical analysis is evaluated from different points of view including: linear buckling analysis, stationary analysis with axial and shear loading. The safety factors are calculated for several designs with different materials (brittle and ductile materials). The results obtained from FEM mechanical analysis for the various electrodes prototypes are presented, which provide guidelines for different electrode designs and

material choice. A proposed fabrication process along with an estimated fabrication cost is also introduced.

A Survey on Deep Learning Classification Algorithms for Motor Imagery

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In recent years, motor imagery electroencephalography decoding has become a promising research field in brain-computer interface. Motor imagery signals generated from the brain can be decoded into certain commands to control external devices. The application of some deep learning algorithms to motor imagery has shown good performance by increasing accuracy and stability, as deep learning can easily handle high-dimensional, non-linear, and non-stationary electroencephalogram data. In this paper, we reviewed trends and approaches of deep learning algorithms for motor based on previously published papers indexed in Web of Science. We screened thirty-six research papers of the motor imagery classification using deep learning methods in the period between 2010 and 2020. In addition, we found the closest terms of the study using the network visualization technique and word cloud. This paper summarizes different input formulation methods used for developing deep learning models. Finally, some suggestions and recommendations for future research on motor imagery classification have been proposed.

Design of a High Efficiency WLED Driver in 40 nm CMOS Technology

Hani H Ahmad and Fadi R. Shahroury

A DC-DC boost-converter-based, three-string White LED (WLED) driver with pure combinational logic in the forward voltage compensation circuit is presented. The proposed architecture optimizes efficiency with the presence of different forward voltage drop across each WLED connected in series in one string and among different strings. The strings don't even need to be balanced (could have different numbers of WLEDs per string). The efficiency optimization is done via setting the minimum proper voltage (in real-time) at the output of the boost converter that activates all parallel strings and by choosing the appropriate arrangement of strings (number of strings and number of WLEDs in each string). Each string has a constant regulated current of 25 mA to drive the series-connected WLEDs in that string. An efficiency of 88:85 % was achieved with input voltage ranges between 3 V to 3:8 V and output voltage up to 25 V. The circuit is implemented using a 40 nm TSMC CMOS process.

A Low Power CMOS Operational Transconductance Amplifier with Improved CMRR

Nedson Maia, Arnaldo Sanchez, Robson Moreno, Tales Cleber Pimenta and Luis H. C. Ferreira

This work proposes a new low power Operational Transconductance Amplifier (OTA) topology. The rejection to common-mode signals is achieved by adding parallel transistors to input MOS transistors in order to increase the Common Mode Rejection Ratio (CMRR). It achieves a gain of 87.34 dB at 9.65 µW power consumption. The article presents a comparison to other OTA topologies. The proposed OTA was designed for the IBM 0.13 µm CMOS technology.